Abstracts

Time delay considerations in high-frequency phase-locked loops

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The time-delayed phase-locked loop (PLL), model predicts drastically different behavior not accounted for in a conventional PLL model. Three results in particular are identified. A critical gain exists for which the equilibrium point becomes a limit cycle. An optimal gain exists that minimizes the acquisition time of the PLL to an external signal. Finally, changes in stability occur first at zero frequency detuning for a given gain and time delay. Verification of this behavior in a 1.5 GHz PLL with reasonable circuit parameter values is demonstrated.

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